AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device having a System in Package structure in which a system comprises:

a wiring substrate;

a microcomputer chip; and

a memory chip, said microcomputer chip and said memory chip being mounted over an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed as a multiport device including an interface between said microcomputer chip and another part of said system including said memory chip and an interface between said microcomputer chip and outside of said system,

wherein said memory chip is constructed to be accessed from the outside of said system via said microcomputer chip,

wherein said microcomputer chip has a substantially square planar shape,

wherein said memory chip has a substantially rectangular planar shape with a long side having a greater length than a side thereof adjacent to the long side,

wherein a length of a side of said microcomputer chip is shorter than a length of the long side of said memory chip, and

wherein said microcomputer chip is mounted over said wiring substrate in a state being stacked over said memory chip such that said microcomputer chip covers a portion of the long side of said memory chip and covers no portion of the side of said memory chip adjacent to the long side.

2. (Previously Presented) The semiconductor device according to claim 1, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, said memory chip is connected to second electrodes of said wiring substrate via a plurality of bonding wires or a plurality of bump electrodes, and said first electrodes are arranged toward an outer periphery of said wiring substrate from said second electrodes.

3. (Previously Presented) The semiconductor device according to claim 1, wherein said memory chip includes a DRAM or a flash memory.

4-5. (Cancelled)

6. (Currently Amended) A semiconductor device having a System in Package structure in which a system comprises:

a wiring substrate;

a microcomputer chip; and

two memory chips, said microcomputer and said memory chips being mounted over an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed as a multiport device including an interface between said microcomputer chip and another part of said system including said two memory chips and an interface between said microcomputer chip and outside of said system,

wherein each of said two memory chips is constructed to be accessed from the outside of said system via said microcomputer chip,

wherein said microcomputer chip has a substantially square planar shape,

wherein each of said two memory chips has a substantially rectangular planar shape with a long side having a greater length than a side thereof adjacent to the long side,

wherein a length of a side of said microcomputer chip is shorter than a length of the long side of each of said two memory chips, and

wherein said two memory chips are mounted over said wiring substrate in a state in which one of said memory chips is stacked over the other, and said microcomputer chip is mounted over said wiring substrate in a state of being stacked over said two memory chips such that said microcomputer chip covers portions of said long sides of said memory chips and covers no portions of the sides of said memory chips adjacent to said long sides.

7. (Previously Presented) The semiconductor device according to claim 6, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, a lower memory chip of said two memory chips is connected to second electrodes of said wiring substrate via a plurality of bump electrodes, an upper memory chip of said two memory chips is connected to third electrodes of said wiring substrate via a plurality of bonding wires, and said first electrodes are arranged toward an outer periphery of said wiring substrate from said second and third electrodes.

8. (Previously Presented) The semiconductor device according to claim 6, wherein one of said two memory chips includes a DRAM, and the other includes a flash memory.

9. (Previously Presented) The semiconductor device according to claim 6, wherein a lower surface of said wiring substrate is formed with a plurality of bump electrodes constructing external connection terminals.

10. (Previously Presented) The semiconductor device according to claim 1, wherein said microcomputer chip and said memory chip have respective terminals, a number of terminals of said microcomputer chip being much greater than a number of terminals of said memory chip.

11. (Previously Presented) The semiconductor device according to claim 10, wherein the terminals of said memory chip are arranged such that they are not superposed over the terminals of said microcomputer chip in a plan view.

12. (Previously Presented) The semiconductor device according to claim 7, wherein an under-fill resin is filled in a gap between said lower memory chip and said wiring substrate.